In the Specification

The specification has been amended as follows:

Please delete paragraph [0007] beginning on page 2 and replace it with the following paragraph:

[0007] As the demand for higher performance integrated circuits dictates smaller critical dimension feature sizes with shallower implant junction depths and ever thinner MOSFET gate films, the use of FIB processing will also increase. Currently, a number of techniques exist in the art for electron holography and sample preparation using FIB microscopy for transmission electron microscopy (TEM). However, the art is deficient in TEM holography techniques to verify site-specific defects in sub-micron devices, i.e., 130nm and smaller, due to limitations in electrical characterization isolation, sample surface preparation methods and requirements for uniformity thickness.

Please delete paragraph [0042] beginning on page 8 and replace it with the following paragraph:

[0042] Once the specific site(s) of any sub-micron defects are electrically localized to either the drain or source side of the MOSFET, a top layer, or alternatively a plurality of top layers of the MOSFET device are removed to expose an underlying metal layer over at least one electrical body contact 20 of the MOSFET device in need of repair, editing or the like. Depending on the

layout of the ULSI MOSFET, the removal of the top layers of the MOSFET device may ~~involving~~ involve stopping at a metallization level 30 that is at least one level, as shown in Fig. 1A, above the level of the polysilicon gate, therein isolating it from plasma charges, accelerating ion beams, as well as gallium ions, xenon difluoride gas chemistries, bromine gas chemistries (associated with FIB) in these charge sensitive MOSFET devices and the like. Alternatively, as shown in Fig. 1B, the top layers of the MOSFET may be removed, therein stopping at a metal ~~layers~~ layer 50 that is several metal layers above the level of the polysilicon gate.

Please delete paragraph [0050] beginning on page 11 and replace it with the following paragraph:

[0050] In the electrical probing step of the invention, a plurality of conductive wiring connections ~~70are~~ 70 are then formed, preferably by FIB CVD, in a direction that is away from the sensitive underlying region of the MOSFET device to be analyzed by TEM, as shown in the top plan representative views of Figs. 2A and 2B. These conductive wiring connections 70 connect the thin conductive film 90 within openings 85 to a distant, larger conductive pad region 75 that resides on the protective cap layer 80 to permit electrical probing. In the present invention, by depositing the thin conductive film 90 on sidewalls of openings 85, and connecting such conductive film 90 to large conductive probe pad region(s) 75 via the conductive connectors 70, the risks of charge

buildup, gallium ion implantation and silicon amorphous damage are significantly reduced.

Please delete paragraph [0059] beginning on page 14 and replace it with the following paragraph:

[0059] An essential feature of the invention is that the MOSFET device is affixed with high temperature silicone or equivalent grease (for heat transfer characteristics) to the carbon planchet fixture 120, which in turn, is affixed to a liquid cooled rotating, tilting stage. Once the noble gas collimated ion beam incremental milling of the first surface area of the MOSFET is complete, this liquid cooled rotating tilting stage permits the formation of a thin conductive coating of carbon122 on the planar milled first surface. Once this first surface is ion milled, the TEM grid attached to the sample is flipped over and the second surface is similarly exposed to the noble gas collimated ion beam for incremental milling to remove gallium contamination and silicon ~~amporhization~~ amorphization surface damage caused by the FIB. During this second-side milling step, the sample is similarly affixed with high temperature silicon or equivalent grease (for heat transfer characteristics) to the carbon planchet fixture 120, which in turn, is affixed to a liquid cooled rotating tilting stage. This thin coating of carbon preferably has a thickness ranging from about 75 angstroms to about 150 angstroms, more preferably, the thin carbon coating is less than about 100 angstroms thick. This conductive coating on the

surfaces of the MOSFET is essential for subsequent holographic imaging of the defective regions of the MOSFET device.